

PATENT NUMBER

	Class	Subclass
ISSUE CLASSIFICATION		

O.I.P.E. SCANNED <i>LM</i> Q.A. <i>TM</i>	PATENT DATE
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APPLICATION NO. 09/922479	CONT/PRIOR F	CLASS 714	SUBCLASS 733	ART UNIT 2133	EXAMINER De cadu
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Thomas Zettler

Method and device for testing an integrated circuit, integrated circuit to be tested, and wafer with a large number of integrated circuits to be tested -

**ISSUING CLASSIFICATION**[illegible]

<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>	<b>DRAWINGS</b>			<b>CLAIMS ALLOWED</b>	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	<div>_____ (Assistant Examiner) _____ (Date)</div> <div>_____ (Primary Examiner) _____ (Date)</div> <div>_____ (Legal Instruments Examiner) _____ (Date)</div>			<b>NOTICE OF ALLOWANCE MAILED</b>	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ <div>_____</div> <div>_____</div>				<b>ISSUE FEE</b>	
				Amount Due	Date Paid
<input type="checkbox"/> The terminal ____ months of this patent have been disclaimed.				<b>ISSUE BATCH NUMBER</b>	
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